Course Code: 23VL3D14

BONAM VENKATA CHALAMAYYA INSTITUTE OF TECHNOLOGY & SCIENCE

(AUTONOMOUS)

II - M.Tech III-Semester Regular Examinations (BR23), Aug/Sep - 2024

DIGITAL SYSTEM DESIGN & VERIFICATION (VLSI)

Time: 3 hours Max. Marks: 75

Answer any Five Questions One Question for One UNIT
ALL the Question Carry Equal Marks

	UNIT-I	Marks	CO	BL
1.a)	Describe the FIFO circuit and its operation. Illustrate any two applications of FIFO circuit in modern digital design.	8M	CO1	L3
b)	Discuss about Programmable counter	7M	CO1	L2
	OR			
2.a)	Describe the Barrel shifter circuit and its operation. Illustrate the application of barrel shifter.	7M	CO1	L3
b)	Differentiate between synchronous reset and asynchronous reset	8M	CO1	L4

	UNIT-II	Marks	CO	BL
3.a)	Write the HDL Program for Asynchronous Counter.	7M	CO2	L2
b)	Illustrate Soft IP, Hard IP, Physical IP	8M	CO2	L3
	OR			
4.a)	Write the VERILOG Program for synchronous Counter.	7M	CO2	L2
b)	Illustrate the Applications of Verilog AMS	8M	CO2	L3

	UNIT-III	Marks	CO	BL
5.a)	Explain Why randomization is important in Functional verification	7M	CO3	L2
b)	Describe the method used to connect the test bench with the design in system Verilog	8M	CO3	L2
	OR			
6.a)	Describe the following system Verilog data types: - i) Different types of arrays in system Verilog ii) Queues	8M	CO3	L2
b)	Illustrate why Perl or any other similar scripting language is important in Chip design flow.	7M	CO3	L3

	UNIT-IV	Marks	CO	BL
7.a)	Discuss the following Process effects in physical design: Antenna Effect & Electro migration	8M	CO4	L2
b)	Discuss the following terminologies: - Placement, Routing and Clock tree synthesis	7M	CO4	L2
	OR			
8.a)	Define IR drop. Describe how IR drop affects the signal integrity	7M	CO4	L2
b)	Illustrate the following with signal integrity issues in connection with physical design: Sources of Noise in layout and Crosstalk in layout.	8M	CO4	L3

	UNIT-V	Marks	CO	BL
9.a)	Explain the functioning of Anti-fuse-based FPGAs, SRAM based FPGAs and EPROM based FPGAs	15M	CO5	L2
	OR			
10.a)	Draw the Architecture of PAL and Explain with one Example	8M	CO5	L3
b)	Draw the Structure of FPGA and Explain each block	7M	CO5	L2

COURSE CO-ORDINATOR

HEAD OF THE DEPT

Head of the Department
Electronics & Communication Engineering
B.V.C. Institute of Technology and
Batlapalem, Amalapuram - 533 201.

BONAM VENKATA CHALAMAYYA INSTITUTE OF TECHNOLOGY & SCIENCE
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DEPARTMENT: ECE **YEAR: MTECH II YEAR III RD SEM**

SUBJECT NAME: DIGITAL SYSTEM DESIGN&VERIFICATION

COURSE OUTCOMES (COS)

C211.1	Analyse the Impact of Combinational and Sequential Circuits, Finite State Machines	ANALYZE
C211.2	Demonstrate a strong foundation in Verilog HDL fundamentals, design, simulation, testbench design and verification of combinational and sequential logic circuits, for effective validation.	UNDERSTAND
C211.3	Apply verification guidelines using System Verilog, including data types, procedural statements, routines, and effective connection of testbenches to designs for robust verification.	APPLY
C211.4	Analyse the current challenges in physical design, Roots of challenges, models, flows, SI Challenges	ANALYZE
C211.5	Understand FPGA structures and the design flows for ASICs, including the steps involved in designing, simulating, and prototyping digital systems using FPGA and ASIC technologies.	UNDERSTAND

Course Coordinator

HOD

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