



**BONAM VENKATA CHALAMAYYA INSTITUTE OF TECHNOLOGY & SCIENCE**  
(AUTONOMOUS)  
(Approved by AICTE, Permanently Affiliated to JNTUK, Kakinada, Accredited by NAAC with 'A' Grade)  
**DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING**

**BR23 B.TECH II YEAR SYLLABUS**

<b>II Year-I Semester</b>					
<b>23EC3T02</b>	<b>SWITCHING THEORY AND LOGIC DESIGN</b>	<b>L</b>	<b>T</b>	<b>P</b>	<b>C</b>
		<b>3</b>	<b>0</b>	<b>0</b>	<b>3</b>

**Course Objectives:**

- To solve a typical number base conversion and analyze new error coding techniques.
- Theorems and functions of Boolean algebra and behavior of logic gates
- To optimize logic gates for digital circuits using various techniques.
- Boolean function simplification using Karnaugh maps and Quine-McCluskey methods
- To understand concepts of combinational circuits.
- To develop advanced sequential circuits.

**UNIT – I : REVIEW OF NUMBER SYSTEMS & CODES**

Representation of numbers of different radix, conversion from one radix to another radix, r- 1's compliments and r's compliments of signed members. Gray code, 4 bit codes; BCD, Excess-3, 2421, 8 4-2-1 code etc. Error detection & correction codes: parity checking, even parity, odd parity, Hamming code.

**BOOLEAN THEOREMS AND LOGIC OPERATIONS**

Boolean theorems, principle of complementation & duality, De-morgan theorems. Logic operations ; Basic logic operations -NOT, OR, AND, Universal Logic operations, EX-OR, EX- NOR operations. Standard SOP and POS Forms, NAND-NAND and NOR-NOR realizations, Realization of three level logic circuits.

**UNIT – II: MINIMIZATION TECHNIQUES**

Minimization and realization of switching functions using Boolean theorems, K-Map (up to 6 variables) and tabular method (Quine-McCluskey method) with only four variables and single function.

**COMBINATIONAL LOGIC CIRCUITS DESIGN:**

Design of Half adder, full adder, half subtractor, full subtractor, applications of full adders; 4- bit adder-subtractor circuit, BCD adder circuit, Excess 3 adder circuit and carry look-a- head adder circuit, Design code converts using Karnaugh method and draw the complete circuit diagrams.

**UNIT – III: COMBINATIONAL LOGIC CIRCUITS DESIGN USING MSI &LSI**

Design of encoder, decoder, multiplexer and de-multiplexers, Implementation of higher order circuits using lower order circuits. Realization of Boolean functions using decoders and multiplexers. Design of Priority encoder, 4-bit digital comparator and seven segment decoder.

**INTRODUCTION OF PLD's**

PLDs: PROM, PAL, PLA -Basics structures, realization of Boolean functions, Programming table.

Dr T S S Phani, Professor & Head of the Department, ECE, BVCITS, Batlapalem	Dr. N V S Narasimha Sarma Professor, Dept of ECE, NIT, Warangal.	Dr.M Rama Subba Reddy, Professor, Dept of Applied Mechanics, IIT Chennai.	Dr. BT Krishna, Professor, Dept of ECE,UCEK,JNTUK, Kakinada,	Dr. M Chakravarthy, Scientist 'F', Head of antenna Directorate, DRDL, DRDO, Hyderabad.	Dr CH V Ravi Sankar Associate professor, Department of ECE, Aditya University, Surampalem.

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**UNIT – IV: SEQUENTIAL CIRCUITS I**

Classification of sequential circuits (synchronous and asynchronous) , operation of NAND & NOR Latches and flip-flops; truth tables and excitation tables of RS flip-flop, JK flip- flop, T flip-flop, D flip-flop with reset and clear terminals. Conversion from one flip-flop to another flip- flop. Design of 5 ripple counters, design of synchronous counters, Johnson counter, ring counter. Design of registers - Buffer register, control buffer register, shift register, bi- directional shift register, universal shift register

Study the following relevant ICs and their relevant functions 7474, 7475, 7476, 7490, 7493, 74121.

**UNIT – V: SEQUENTIAL CIRCUITS II**

Finite state machine; state diagrams, state tables, reduction of state tables. Analysis of clocked sequential circuits Mealy to Moore conversion and vice-versa. Realization of sequence generator, Design of Clocked Sequential Circuit to detect the given sequence (with overlapping or without overlapping)

**TEXT BOOKS:**

1. Switching and finite automata theory Zvi. KOHAVI, Niraj. K.Jha 3rd Edition, Cambridge University Press, 2009
2. Digital Design by M.Morris Mano, Michael D Ciletti, 4th edition PHI publication, 2008
3. Switching theory and logic design by Hill and Peterson, Mc-Graw Hill TMH edition, 2012.

**REFERENCES:**


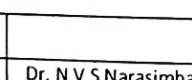
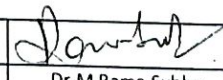
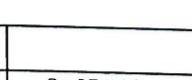
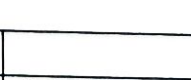

1. Fundamentals of Logic Design by Charles H. Roth Jr, Jaico Publishers, 2006
2. Digital electronics by R S Sedha. S.Chand & company limited, 2010
3. Switching Theory and Logic Design by A. Anand Kumar, PHI Learning Pvt Ltd, 2016.
4. Digital logic applications and design by John M Yarbough, Cengage Learning, 2006.
5. TTL 74-Series data book.

**Online Learning Resources:**

- <https://nptel.ac.in/courses/108/105/108105132/>
- <https://nptel.ac.in/courses/117/106/117106086/>

**Course Outcomes:**

COs	Statements	BL
CO1	Classify different number systems and apply to generate various codes.	BL2
CO2	Use the concept of Boolean algebra in minimization of switching functions	BL3
CO3	Design different types of combinational logic circuits.	BL3
CO4	Apply knowledge of flip-flops in designing of Registers and counters	BL3
CO5	The operation and design methodology for synchronous sequential circuits and algorithmic state machines.	BL3
CO5	Produce innovative designs by modifying the traditional design techniques.	BL4

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