Course Code: 23EC3T02

BONAM VENKATA CHALAMAYYA INSTITUTE OF TECHNOLOGY & SCIENCE

**(AUTONOMOUS)**

***II-B.Tech I-Semester Regular Examinations (BR23), November- 2024***

**SWITCHING THEORY AND LOGIC DESIGN (ECE)**

Time: 3 hours Max. Marks: 70

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*Question Paper consists of Part-A and Part-B*

*Answer **ALL** the question in **Part-AandPart-B***

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PART–A (10X2 = 20M)

| | | Marks | CO | BL |
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| 1. a) | Convert the following.i. $(AB.CD)_{16} = (\ )_{10}$ ii. $(123.321)_8 = (\ )_{10}$ | (2M) | CO1 | BL3 |
| b) | Perform the following subtraction in binary using 1's and 2's complement method: $(677)_{10} - (899)_{10}$ | (2M) | CO1 | BL3 |
| c) | Implement the following function using only NOR gates F=a. (b+ c.d) + (b. c) | (2M) | CO2 | BL3 |
| d) | Design Half Adder and Draw the logic Diagram with its Truth Table | (2M) | CO2 | BL2 |
| e) | Design and implement a two bit comparator using logic gates | (2M) | CO3 | BL2 |
| f) | Design a 1:8 demultiplexer using two 1:4 demultiplexer. | (2M) | CO3 | BL2 |
| g) | What are the differences between Latches and Flip Flops | (2M) | CO4 | BL2 |
| h) | Write the differences between combinational and sequential circuits. | (2M) | CO4 | BL2 |
| i) | Draw the logic diagram of Meelay and Moore models and also explain their operation with examples | (2M) | CO5 | BL2 |
| j) | Explain the procedure of Meelay to Moore conversion. | (2M) | CO5 | BL2 |

PART–B (5X10 = 50M)

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|---|---|---|---|---|
| 2a. | Given the 8 bit data word 01011011, generate the 12 bit composite word for the hamming code that corrects and detects single errors. | 5(M) | CO1 | BL3 |
| b. | Convert the Boolean function F(A,B,C,D) = A+BC+ACD into standard POS form. | 5(M) | CO1 | BL3 |
| | (OR) | | | |
| 3a. | Perform the following addition using excess-3 code i)386+756 ii)254+ 579 | 5(M) | CO1 | BL3 |
| b. | A 7 bit Hamming code is received as 1110101.Is there any error? If yes, locate the position of the error bit. Parity checks are created by odd parity. | 5(M) | CO1 | BL3 |

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| 4a. | Using the Quine–McCluskey tabular method, find the minimum sum of products for F(A,B,C,D,E) =∑m(1,5,6,7,9,13,14,15,17,18,19,21,22,23,25,29,30) | 5(M) | CO2 | BL3 |
| b. | Design a BCD adder circuit and explain its operation | 5(M) | CO2 | BL3 |
| | (OR) | | | |

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|---|---|---|---|---|
| 5a. | Design a circuit to convert BCD code to Excess 3 code using discrete Logic gates. | 5(M) | CO2 | BL2 |
| b. | Simplify the following using K- map and implement the same using NAND gates. Y (A, B, C,D,E) =Σm(0,2,4,5,6,7,11,14,16,20,24,26,29,31) + d(9,12,18,27) | 5(M) | CO2 | BL2 |

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|---|---|---|---|---|
| 6a. | Tabulate the PLA programming table for the four Boolean functions listed below A(x,y,z) = ∑ m(1, 2, 4, 6) B(x,y,z) = ∑m (0, 1, 6, 7) C(x,y,z) = ∑m (2,6) D(x,y,z) = ∑m (1, 2, 3, 5, 7) | 5(M) | CO3 | BL3 |
| b. | Realize the function f(A,B,C,D) = Σ (1,3,4,6,7,8,10,13,15) using i) 16:1 MUX ii) 8:1 MUX | 5(M) | CO3 | BL3 |
| | (OR) | | | |
| 7a. | Implement the following functions using a PROM i) F(w,x,y,z)=Σ(1,9,12,15) ii) G(w,x,y,z)= Σ(0,1,2,3,4,5,7,8,10,11,12,13,14,15) | 5(M) | CO3 | BL3 |
| b. | Define decoder. Construct IC74LS138 decoder using logic gates and truth table | 5(M) | CO3 | BL2 |

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|---|---|---|---|---|
| 8a. | Draw the logic diagram of a SR latch using NOR gates. Explain its Operation using excitation table | 5(M) | CO4 | BL2 |
| b. | Convert D flip-flop into T and JK flip-flops. | 5(M) | CO4 | BL2 |
| | (OR) | | | |
| 9a. | Draw and explain the logic diagram for a 4-bit binary ripple down counter using positive edge triggered flip-flops | 5(M) | CO4 | BL2 |
| b. | Draw a 4-bit bi-directional shift register logic diagram and explain its operation | 5(M) | CO4 | BL2 |

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|---|---|---|---|---|
| 10a. | Reduce the number of states in the following state table and tabulate the reduced state table. | 10(M) | CO5 | BL3 |
| | (OR) | | | |
| 11a | Convert the following Mealy machine into a corresponding Moore machine: | | | |

| PS | NS, O/P | |
|---|---|---|
| | X=0 | X=1 |
| a | f, 0 | b, 0 |
| b | d, 0 | c, 0 |
| c | f, 0 | e, 0 |
| d | g, 1 | a, 0 |
| e | d, 0 | c, 0 |
| f | f, 1 | b, 1 |
| g | g, 0 | h, 1 |
| h | g, 1 | a, 0 |

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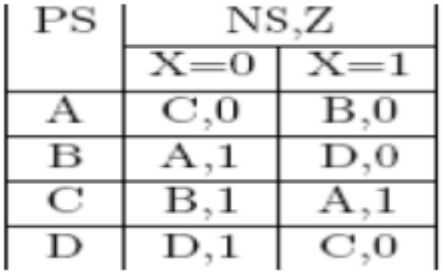
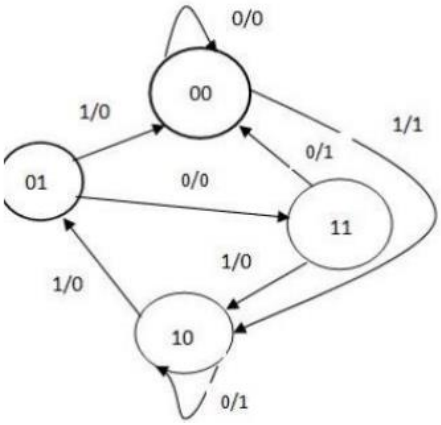
|---|---|---|---|---|
| |  | 5(M) | CO5 | BL3 |
| b. | A sequential circuit has one input and one output .The state diagram is shown below. Design the sequential circuit with D flip-flops  | 5(M) | CO5 | BL3 |

| PS | NS,Z | |
|---|---|---|
| | X=0 | X=1 |
| A | C,0 | B,0 |
| B | A,1 | D,0 |
| C | B,1 | A,1 |
| D | D,1 | C,0 |



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