Course Code: 23VL1D07

BONAM VENKATA CHALAMAYYA INSTITUTE OF TECHNOLOGY & SCIENCE

(AUTONOMOUS)

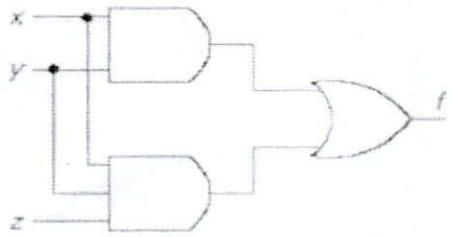
I - M. Tech II-Semester Regular Examinations (BR23), July/Aug - 2025

Design for Testability (VLSI)

Time: 3 hours | Max. Marks: 75

Answer any Five Questions One Question for One UNIT
ALL the Question Carry Equal Marks

	UNIT-I	**Marks**	**CO**	**BL**
1.a)	Make use of single stuck at fault model to find faults in digital circuits.	8M	CO1	Analyze
b)	Find test vector to test S-A-0 fault at node z in Fig.1(a) using Boolean Difference method.	7M	CO1	Evaluate



OR

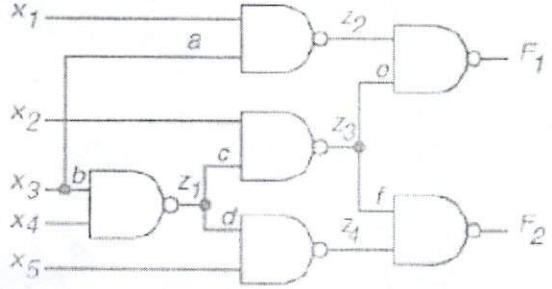
2.a)	How structural testing is used to detect the faults in the circuit? Compare it with functional testing.	7M	CO1	Analyze
b)	Why testing is needed? Classify testing methods?	8M	CO1	Analyze

	UNIT-II	**Marks**	**CO**	**BL**
3.a)	Write the Compiled code simulation algorithm and examine how it is effective for zero level combinational logic?	7M	CO2	Create
b)	Explain concurrent and parallel fault simulation.	8M	CO2	Under stand

OR

4.a)	Explain different Modelling Circuits for Simulation with one example	7M	CO2	Under stand
b)	Explain about the true-value simulation algorithms in details.	8M	CO2	Under stand

	UNIT-III	**Marks**	**CO**	**BL**
5.a)	For the circuit shown in figure, compute the combinational SCOAP testability measures, both controllability and observability.	8M	CO3	Anal yze



b)	Describe about Full scan LSSD and partial scan LSSD with suitable diagrams	7M	CO3	Anal yse

OR

6.a)	Explain the different High Level Testability Measures of a DFT in detail	7M	CO3	Analyse
b)	Develop the design guidelines for Ad-Hoc DFT and write its advantages and disadvantages.	8M	CO3	Evaluate

	UNIT-IV	**Marks**	**CO**	**BL**
7.a)	Explain in detail March-C algorithm with all steps used for MBIST	7M	CO4	Evaluate
b)	Examine how circular self-test path system minimizing the test schedule complexity?	8M	CO4	Analyse

OR

8.a)	Build a typical BIST architecture and explain about each block.	7M	CO4	Understand
b)	Draw the block diagram for a BIST implementation using BILBO and explain the test procedure	8M	CO4	understand

	UNIT-V	**Marks**	**CO**	**BL**
9.a)	Examine the different BDSL Description Components in detail	7M	CO5	Understand
b)	Describe the various JTAG TAP controller test instructions along with timing waveforms.	8M	CO5	Analyze

OR

10.a)	Describe about JTAG testing features.	7M	CO5	Understand
b)	Analyse how boundary scan testing method is used to test the core of IC?	8M	CO5	Analyze

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