Course Code: 23AD5T02

BONAM VENKATA CHALAMAYYA INSTITUTE OF TECHNOLOGY &SCIENCE

(AUTONOMOUS)

III B.Tech I Semester Regular Examinations (BR23), SEP - 2025

COMPUTER ORGANIZATION AND ARCHITECTURE

CSE-(AI &DS)

Time: 3 hours Max. Marks: 70

Question Paper consists of Part-A and Part-B

*Answer **ALL** the question in **Part-A and Part-B***

PART–A (10X2 = 20M)

		Marks	CO	BL
1a)	Give the functional units of a computer.	(2M)	CO1	BL2
b)	Convert the following numbers binary to decimal. $(1011)_2 \rightarrow (?)_{10}$	(2M)	CO1	BL2
c)	Discuss about latches and flip-flops.	(2M)	CO2	BL2
d)	Describe multi bit adder.	(2M)	CO2	BL1
e)	Discuss computer instructions.	(2M)	CO3	BL2
f)	Explain shift and rotate micro operations.	(2M)	CO3	BL4
g)	Define control memory.	(2M)	CO4	BL2
h)	Illustrate the micro program with an example.	(2M)	CO4	BL3
i)	Differentiate between RAM and ROM.	(2M)	CO5	BL4
j)	Define input-output interface.	(2M)	CO5	BL2

PART–B (5X10 = 50M)

2a.	Explain about hamming code for error correction.	5(M)	CO1	BL4
b.	Classify the numbering system.	5(M)	CO1	BL3
	(OR)			
3a.	Derive K-Map representation and simplify the 3-variable K-Map $\Sigma m(0,1,5,7)$.	5(M)	CO1	BL3
b.	Explain about fixed point representation with an example.	5(M)	CO1	BL3

4a.	Explain combinational circuit and design procedure.	5(M)	CO2	BL4
b.	Illustrate briefly about 4X1 multiplexers.	5(M)	CO2	BL3
	(OR)			
5.	Explain about ripple counters using T flip-flops.	10(M)	CO2	BL4

6a.	Discuss about addition and subtraction algorithms with sign magnitude data.	5(M)	CO3	BL2
b.	Discriminate the Booth multiplication algorithm with an example.	5(M)	CO3	BL4
	(OR)			
7a.	Draw the bus structure of computers.	5(M)	CO3	BL3
b.	With a neat Flowchart explain Floating-Point Addition and Subtraction.	5(M)	CO3	BL4

8a.	Draw the design of Control unit with a neat diagram.	5(M)	CO4	BL3
b.	Construct the concept of general register organization in a CPU.	5(M)	CO4	BL3
	(OR)			
9.	Explain the following addressing modes. i) Index mode ii) Auto increment mode iii) Auto decrement mode.	10(M)	CO4	BL4

10.	Explain about memory hierarchy.	10(M)	CO5	BL4
	(OR)			
11a	Demonstrate short notes on secondary storage devices.	5(M)	CO5	BL3
b.	Generalize the concept of cache memory.	5(M)	CO5	BL2

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Faculty Signature

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Head of the Department

Head of the Dept.
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