Course Code: **23CS5E02**

BONAM VENKATA CHALAMAYYA INSTITUTE OF TECHNOLOGY & SCIENCE

(AUTONOMOUS)

III–B.Tech.I – Semester Regular Examinations (BR23), Nov/Dec– 2025

COMPUTER ORGANIZATION AND ARCHITECTURE (ECE)

Time: 3 hours Max. Marks: 70

Question Paper consists of Part-A and Part-B

*Answer **ALL** the question in **Part-AandPart-B***

PART–A (10X2 = 20M)

		Marks	CO	BL
1. a)	Write a short note on three-state buffer.	(2M)	CO 1	2
b)	Differentiate between computer organization and computer architecture.	(2M)	CO 1	2
c)	Define the categories of computer programs.	(2M)	CO 2	2
d)	Define Instruction Code.	(2M)	CO 2	2
e)	Explain types of interrupts.	(2M)	CO 3	2
f)	Explain any 2 addressing modes.	(2M)	CO 3	2
g)	What is meant by hand shaking.	(2M)	CO 4	2
h)	What do you mean by FIFO buffer.	(2M)	CO 4	2
i)	Explain Hit rate and Miss penalty	(2M)	CO 5	2
j)	Compare cache and main memory.	(2M)	CO 5	2

PART–B (5X10 = 50M)

2a.	With the help of block diagram explain 4-bit arithmetic circuit.	10M	CO 1	2
	(OR)			
3a.	Discuss the functional units of a digital computer with block diagram.	10M	CO 1	2
4a.	Draw and explain about the instruction cycle state diagram	10M	CO 2	2
	(OR)			
5a.	Explain about microinstruction format in detail.	10M	CO 2	2
6a.	With an example, explain the concept of one-address, two-address, three-address and zero-address instructions.	10M	CO 3	2
	(OR)			
7a.	Explain the booths algorithm for signed multiplication.	10M	CO 3	2
8a.	Explain IO interface with an example.	10M	CO 4	2
	(OR)			
9a.	Describe the organization of DMA.	10M	CO 4	2
10a.	Draw and explain the block diagram of RAM and ROM chips.	10M	CO 5	2
	(OR)			
11a.	Discuss about direct mapping and set associative mapping.	10 M	CO 5	2

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