Course Code: 23EE5T07

BONAM VENKATA CHALAMAYYA INSTITUTE OF TECHNOLOGY & SCIENCE

(AUTONOMOUS)

III - B. Tech I-Semester Regular Examinations (BR23), Nov/Dec - 2025

DIGITAL CIRCUITS (EEE)

Time: 3 hours Max. Marks: 70

Question Paper consists of Part-A and Part-B

*Answer **ALL** the question in **Part-A andPart-B***

PART–A (10X2 = 20M)

		Marks	CO	BL
1. a)	Define K-map?	(2M)	CO1	BL4
b)	What is a Look ahead Carry Generator?	(2M)	CO1	BL2
c)	Implement F(A,B,C)= ∑m(0,1,3,5) using 8:1 Multiplexer?	(2M)	CO2	BL3
d)	What is Priority Encoder?	(2M)	CO2	BL1
e)	What is the Disadvantage of SR Filp Flop?	(2M)	CO3	BL1
f)	What is Race Around Condition?	(2M)	CO3	BL1
g)	What is meant by Redundant states?	(2M)	CO4	BL1
h)	Differentiate between Synchronous and Asynchronous Sequential Circuits?	(2M)	CO4	BL2
i)	Define Fan in and Fan out?	(2M)	CO5	BL4
j)	Define Propagation Delay time?	(2M)	CO5	BL4

PART–B (5X10 = 50M)

2a.	Simplify the following Boolean function, using three-variable maps: F(x, y,z) = ∑(0,2,6,7)	5M	CO1	BL4
b.	Explain a four-bit binary adder circuit with relevant diagram.	5M	CO1	BL2
	(OR)			
3a.	Design BCD Adder Circuit?	10M	CO1	BL6

4a.	Design 7 Segment Decoder?	10M	CO2	BL6
	(OR)			
5a.	Using PLA with 3 Inputs, 4 AND Gates and Two Outputs to implement the following Boolean function F1(A, B, C) = ∑m (3,5,6,7) and F2(A, B, C) = ∑m (1,2,3,4)	10M	CO2	BL3

6a.	Explain the designing procedure of Master Slave JK Flip-Flop with suitable diagram?	5M	CO3	BL2
b.	Convert JK Flip Flop to T Flipflop?	5M	CO3	BL3

	(OR)			
7	Design 4 bit Asynchronous Counter using JK Flip-Flops?	10M	CO3	BL6

8a.	What is the importance of reduction of number of states? What is the advantage of standard form for state tables? Explain with an example.	5M	CO4	BL1
b.	Explain the design procedure of Asynchronous sequential circuits.	5M	CO4	BL2
	(OR)			
9a.	Design a Sequence detector to detect the sequence 11010 Using T flip Flops?	10M	CO4 CO4	BL6

10a.	Explain DC Noise Margin with reference to TTL Gate?	5M	CO5	BL2
b.	Design CMOS Transistor Circuit for 2 Input AND gate?	5M	CO5	BL6
	(OR)			
11a.	Which of the parameters decide the Fan Out and How?	10M	CO5	BL1

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