Course Code: 23VL3D14

BONAM VENKATA CHALAMAYYA INSTITUTE OF TECHNOLOGY & SCIENCE

(AUTONOMOUS)

II - M. Tech I-Semester Regular/Supplementary Examinations (BR23), Dec - 2025

DIGITAL SYSTEM DESIGN & VERIFICATION (VLSI)

Time: 3 hours Max. Marks: 75

Answer any Five Questions One Question for One UNIT
ALL the Question Carry Equal Marks

	UNIT-I	**Marks**	**CO**	**BL**
1.a)	Identify two logic families commonly used in digital circuits. What is the typical power dissipation of a CMOS gate?	7M	1	1
b)	Differentiate between TTL and CMOS logic families in terms of power consumption.	8M	1	2
	OR			
2.a)	Implement a 4-bit programmable counter that can count up or down based on an external signal.	7M	1	3
b)	Explain how a 4-to-1 multiplexer works. Illustrate the function of an encoder with an example.	8M	1	2
	UNIT-II	**Marks**	**CO**	**BL**
3.a)	What is the primary difference between Verilog and VHDL? Define RTL in the context of Verilog HDL.	7M	2	1
b)	Describe the role of a test bench in verifying a Verilog module.	8M	2	2
	OR			
4.a)	Develop a Verilog module to compare two 4-bit numbers and indicate which one is larger.	7M	2	3
b)	Write a Verilog module to implement a shift register with parallel load capability and simulate its functionality.	8M	2	3
	UNIT-III	**Marks**	**CO**	**BL**
5.a)	Differentiate between static and dynamic data types in System Verilog.	7M	3	2
b)	Describe the purpose of fault models in testing digital circuits.	8M	3	2
	OR			
6.a)	Write a System Verilog assertion to detect whether a signal remains high for more than 3 clock cycles.	7M	3	3
b)	Write the advantages and limitations of using JTAG for debugging a complex digital circuit.	8M	3	2
	UNIT-IV	**Marks**	**CO**	**BL**
7.a)	Explain the significance of wire load models in addressing delay issues in physical design.	7M	4	2
b)	Analyse the trade-offs between wire width, spacing, and delay in high-performance designs.	8M	4	4
	OR			
8.a)	Compare the influence of process variations on different stages of the PD flow and suggest mitigation strategies.	7M	4	4

		Marks	CO	BL
b)	Design a simple experiment to analyse crosstalk noise between two adjacent wires at different spacings.	8M	4	3
	UNIT-V	**Marks**	**CO**	**BL**
9.a)	Explain the difference between PROM, PLA, and PAL in terms of structure and functionality.	7M	5	2
b)	Write a Verilog code for configuring an SRAM-based FPGA to implement a 4-bit counter.	8M	5	3
	OR			
10.a)	Evaluate the advantages and disadvantages of coarse-grained reconfigurable devices compared to traditional ASICs.	7M	5	4
b)	Outline the steps in the ASIC design flow and explain where FPGAs fit in the flow.	8M	5	2

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