III Year-II Semester					
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23EC6T09	VLSI DESIGN	3	0	0	3

Course Outcomes:
- Demonstrate a clear understanding of CMOS fabrication flow and technology scaling.[BL2]
- Design MOSFET based logic circuit and apply scaling principles and limitations.[BL4]
- Design basic building blocks in Analog IC design.[BL4]
- Design various CMOS logic circuits for design of Combinational logic circuits. [BL4]
- Distinguish among various FPGA technologies and families, emerging device technologies. . [BL4]

UNIT-I:
INTRODUCTION AND BASIC ELECTRICAL PROPERTIES OF MOS CIRCUITS: VLSI Design Flow, Introduction to IC technology, Fabrication process: nMOS, pMOS and CMOS. I_{ds} versus V_{ds} Relationships, Aspects of MOS transistor Threshold Voltage, MOS transistor Trans, Output Conductance and Figure of Merit. nMOS Inverter, Pull-up to Pull-down Ratio for nMOS inverter driven by another nMOS inverter, and through one or more pass transistors. Alternative forms of pull-up, The CMOS Inverter, Latch-up in CMOS circuits, Bi-CMOS Inverter, Comparison between CMOS and BiCMOS technology, MOS Layers, Stick Diagrams, Design Rules and Layout, Layout Diagrams for MOS circuits.
(TEXT BOOK-1, TEXT BOOK-4)   14Hrs

UNIT-II:
BASIC CIRCUIT CONCEPTS: Sheet Resistance, Sheet Resistance concept applied to MOS transistors and Inverters, Area Capacitance of Layers, Standard unit of capacitance, some area Capacitance Calculations, The Delay Unit, Inverter Delays, driving large capacitive loads, Propagation Delays, Wiring Capacitances, Choice of layers.
SCALING OF MOS CIRCUITS: Scaling models and scaling factors, Scaling factors for device parameters, Limitations of scaling, Limits due to sub threshold currents, Limits on logic levels and supply voltage due to noise and current density.
(TEXT BOOK-1, TEXT BOOK-4)   10Hrs

UNIT-III:
BASIC BUILDING BLOCKS OF ANALOG IC DESIGN: Regions of operation of MOSFET, Modelling of transistor, body bias effect, biasing styles, single stage amplifier with resistive load, single stage amplifier with diode connected load, Common Source amplifier, Common Drain amplifier, Common Gate amplifier, current sources and sinks.
(TEXT BOOK-1, TEXT BOOK-3,TEXT BOOK-4)   10Hrs
UNIT-IV:
CMOS COMBINATIONAL AND SEQUENTIAL LOGIC CIRCUIT DESIGN:
Static CMOS Design: Complementary CMOS, Rationed Logic, Pass-Transistor Logic, design of Half adder, full adder, multiplexer, decoder.

Dr. T.S. PHANI
B.E, M.Tech Ph.D, MIETE, MIAENG
Professor & HOD
Department of ECE
BVCITS, Batlapalem

Dynamic CMOS Design: Dynamic Logic-Basic Principles, Speed and Power Dissipation of Dynamic Logic, Issues in Dynamic Design, Cascading Dynamic Gates, Design examples of sequential circuits: Cross coupled NAND and NOR flipflops, D flipflop, SR JK flip flop, SR Master Slave flip flop.
(TEXT BOOK-1, TEXT BOOK-4)   16Hrs

UNIT-V:
FPGA DESIGN: FPGA design flow, Basic FPGA architecture, FPGA Technologies, Introduction to FPGA Families.

INTRODUCTION TO ADVANCED TECHNOLOGIES: Giga-scale dilemma, Short channel effects, High–k, Metal Gate Technology, FinFET, TFET.
(TEXT BOOK-1, TEXT BOOK-4, REFERENCE-2, REFERENCE-3)   10Hrs

TEXTBOOKS:
1. Essentials of VLSI Circuits and Systems - Kamran Eshraghian, Douglas and A. Pucknell
2. And Sholeh Eshraghian, Prentice-Hall of India Private Limited, 2005 Edition.
3. Design of Analog CMOS Integrated Circuits by Behzad Razavi, McGraw Hill, 2003
4. Digital Integrated Circuits, Jan M. Rabaey, Anantha Chandrakasan and Borivoje Nikolic, 2nd edition, 2016.

REFERENCES:
1. "Introduction to VLSI Circuits and Systems", John P. Uyemura, John Wiley & Sons, reprint 2009.
2. Integrated Nanoelectronics: Nanoscale CMOS, Post-CMOS and Allied Nanotechnologies Vinod Kumar Khanna, Springer India, 1st edition, 2016.
3. FinFETs and other multi-gate transistors, ColingeJP, Editor New York, Springer, 2008.

LINKS:

1. https://ocw.mit.edu/courses/6-012-microelectronic-devices-and-circuits-fall-2009/pages/lecture-notes/
2. https://www.electronics-tutorials.ws/transistor/tran_8.html
3. https://eceagmr.wordpress.com/wp-content/uploads/2014/08/cmos-unit4-uk.pdf
4. https://nptel.ac.in/courses/117101058
5. https://jccluque.wordpress.com/wp-content/uploads/2016/09/capitulo6.pdf
6. https://cds.cern.ch/record/1100537/files/p231.pdf

Dr. T.S.S. PHANI
B.E, M.Tech, Ph.D, MIETE, MIAENG
Professor & HOD
Department of ECE
BVCITS, Batlapa