

Question Paper consists of Part-A and Part-B
Answer ALL the question in Part-A and Part-B

PART-A (10X2 = 20M)

	Marks	CO	BL
1. a) What are universal gates	(2M)	CO1	BL2
b) What are the advantages of carry look ahead adder.	(2M)	CO1	BL2
c) Compare PAL and PLA in terms of programmability and flexibility.	(2M)	CO2	BL3
d) What is higher order demultiplexing?	(2M)	CO2	BL2
e) Differentiate synchronous and asynchronous counters	(2M)	CO3	BL2
f) What are the applications of registers.	(2M)	CO3	BL2
g) Explain the purpose of constructing a state diagram.	(2M)	CO4	BL2
h) What are the essential steps in the analysis of a clocked sequential circuit?	(2M)	CO4	BL2
i) Draw CMOS inverter.	(2M)	CO5	BL3
j) Define power dissipation in Digital circuits	(2M)	CO5	BL2

PART-B (5X10 = 50M)

2a. Implement the Boolean function $F(A, B, C, D) = A'B' + C'D' + B'C'$ using the following two-level gates i) NAND-AND ii) NOR-OR. (OR)	10M	CO1	BL4
3a. Design a full subtractor using NAND gates	10M	CO1	BL3
4a. What is a multiplexer? Design a 4*1 multiplexer. Write the truth table and draw the logic diagram.	5M	CO2	BL3
b. What is a PLD? Tabulate the comparisons between PLA, PAL and PROM. (OR)	5M	CO2	BL2
5a. Design a PAL for the following logical functions. $Y1 = AB + A'CB'$, $Y2 = AB'C + AB + AC'$, $Y3 = AB + BC + CA$	10M	CO2	BL4
6a. Draw the circuit diagram of clocked D-flip-flop with NAND gates and explain its operation using truth table. Give its timing diagram.	5M	CO3	BL3
b.	5M	CO3	BL3

What is a shift register? Explain about the following modes of operations in a four-bit shift register (i) shift right (ii) shift left (iii) bidirectional.

(OR)

7 Design a synchronous 3 bit up-down counter using JK flip flops. 10M CO3 BL4

8a. Explain Melay state machine with state diagram. 5M CO4 BL4

b. What are the capabilities and limitations of finite state machines? Discuss. 5M CO4 BL2

(OR)

9. Reduce the number of states in the following state table using an implication table method and tabulate the reduced state-table. 10M CO4 BL4

PS	NS		Output	
	X=0	X=1	X=0	X=1
A	F	B	0	0
B	D	C	0	0
C	F	E	0	0
D	G	A	1	0
E	D	C	0	0
F	F	B	1	1
G	G	H	0	1
H	G	A	1	0

10a. Explain propagation delay time? 5M CO5 BL2

b. Design CMOS Transistor Circuit for 2 Input NAND gate 5M CO5 BL4

(OR)

11a. Explain ECL logic family with an example 10M CO5 BL4
