

**BONAM VENKATA CHALAMAYYA INSTITUTE OF TECHNOLOGY & SCIENCE
(AUTONOMOUS)**

II-B. Tech I-Semester Supplementary Examinations (BR23), Mar - 2026

DIGITAL LOGIC & COMPUTER ORGANIZATION (CSE&IT)

Time: 3 hours

Max. Marks: 70

*Question Paper consists of Part-A and Part-B
Answer ALL the question in Part-A and Part-B*

PART-A (10X2 = 20M)

	Marks	CO	BL
1. a) Convert $(12.125)_{10}$ into binary.	(2M)	CO1	BL2
b) What are the advantages and disadvantages of K Maps	(2M)	CO1	BL1
c) Define a latch and flip-flop.	(2M)	CO2	BL1
d) Explain the concept of bidirectional shift register	(2M)	CO2	BL2
e) What is signed-operand multiplication?	(2M)	CO3	BL1
f) What is carry propagation?	(2M)	CO3	BL1
g) What is the need of virtual memory	(2M)	CO4	BL1
h) What are the different types of semiconductor memories	(2M)	CO4	BL1
i) What is isolated I/O?	(2M)	CO5	BL1
j) What is interrupt latency?	(2M)	CO5	BL1

PART-B (5X10 = 50M)

2a. Convert the decimal numbers 250.5, 12.0625, 673.23 to binary, base 8 and base 16	5(M)	CO1	BL2
b. How are binary codes classified? Briefly explain each code with suitable examples	5(M)	CO1	BL2
(OR)			
3a. Using K-map determine SOP realization of the following $F(w,x,y,z) = \sum m(1,4,8,9,13,14,15) + \sum \phi(2,3,11,12)$.	5(M)	CO1	BL3
b. Demonstrate different number systems used in computers with examples.	5(M)	CO1	BL3
4a. What is a flip-flop? Design basic flip-flop circuit with NAND gates.	5(M)	CO2	BL5
b. Draw and explain 4-bit controlled buffer register.	5(M)	CO2	BL3
(OR)			
5a. Draw and explain the operation of negative edge triggered JK Flip-Flop.	5(M)	CO2	BL3
b. Define a ripple counter. Design a BCD ripple counter.	5(M)	CO2	BL5
6a. Explain Booth Multiplication algorithm. Perform multiplication on $(-9) * (-13)$ using Booths Algorithm	5(M)	CO3	BL2
b. Compare hardwired control and microprogrammed control.	5(M)	CO3	BL4
(OR)			
7a. Explain floating-point number representation and operations.	5(M)	CO3	BL2
b. Demonstrate the execution of a computer instruction step by step.	5(M)	CO3	BL3

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| 8a. | What is cache memory? Explain different types of mapping from main memory to cache memory. | 5(M) | CO4 | BL2 |
| b. | Explain about the procedure for mapping the virtual address in memory table. | 5(M) | CO4 | BL2 |
| (OR) | | | | |
| 9a. | What is ROM? List the different types of ROMs. | 5(M) | CO4 | BL2 |
| b. | Describe the memory management requirements in modern computers. | 5(M) | CO4 | BL2 |
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| 10a | How an interrupt is recognized? Explain the interrupt cycle. | 5(M) | CO5 | BL3 |
| b | Illustrate the step-by-step account of actions taken during the DMA. | 5(M) | CO5 | BL3 |
| (OR) | | | | |
| 11a | Discuss about parallel priority interrupt. | 5(M) | CO5 | BL2 |
| b. | Describe the bus structure in computer systems and its role in I/O organization. | 5(M) | CO5 | BL2 |
