

**BONAM VENKATA CHALAMAYYA INSTITUTE OF TECHNOLOGY & SCIENCE  
(AUTONOMOUS)**

*I – M.Tech. I - Semester Regular Examinations (BR25), Feb - 2026*

**ANALOG CMOS CIRCUIT DESIGN (VLSI)**

Time: 3 hours

Max. Marks: 60

*Answer any Five Questions One Question from One UNIT*

*ALL the Questions Carry Equal Marks*

<b>UNIT-I</b>		<b>Marks</b>	<b>CO</b>	<b>BL</b>
1.a)	Explain about Integrated circuit Layout and SPICE Models.	6M	CO1	L2
b)	Draw the Simple MOS Large-Signal Model transistor. Briefly explain each component.	6M	CO1	L3
<b>OR</b>				
2.a)	Explain about the CMOS device Model and Explain about the computer simulation modelling.	6M	CO1	L2
b)	Draw and explain the structure of a basic MOS Capacitor and resistor.	6M	CO1	L3
<b>UNIT-II</b>		<b>Marks</b>	<b>CO</b>	<b>BL</b>
3.a)	Discuss about Illustration of the hierarchy of analog circuits for an operational amplifier.	6M	CO2	L3
b)	Explain Current Sinks and Sources with Current–voltage characteristics.	6M	CO2	L2
<b>OR</b>				
4.a)	Define MOS Switch and Discuss about application of an MOS switch.	6M	CO2	L3
b)	Explain in detail Current and Voltage References and Bandgap Reference.	6M	CO2	L2
<b>UNIT-III</b>		<b>Marks</b>	<b>CO</b>	<b>BL</b>
5.a)	Explain Source follower with example of its role as a buffer and its input-output characteristics.	6M	CO3	L2
b)	Draw and explain Simple folded cascode folded cascode with proper biasing and folded cascode with NMOS input.	6M	CO3	L3
<b>OR</b>				
6.a)	Explain Common-Source Stage with Triode Load and Source Degeneration with neat circuits.	6M	CO3	L4
b)	Explain about Common-Source Stage with Diode-Connected Load with small-signal equivalent circuit.	6M	CO3	L2
<b>UNIT-IV</b>		<b>Marks</b>	<b>CO</b>	<b>BL</b>
7.a)	Discuss about Various types of inverting CMOS amplifiers.	6M	CO4	L3
b)	Explain Statistical Characteristics of Noise with Noise Spectrum and Amplitude Distribution.	6M	CO4	L2

**OR**

- |      |   |    |     |    |
|------|---|----|-----|----|
| 8.a) | Explain Statistical Characteristics of Correlated and Uncorrelated Sources and Signal-to-Noise Ratio. | 6M | CO4 | L2 |
| b)   | Explain about Noise in Single-Stage Amplifiers with Common-Gate Stage.                                | 6M | CO4 | L4 |

**UNIT-V**

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|------|--|--------------|-----------|-----------|
| 9.a) | Discuss about Compensation of Operational Amplifiers with Frequency and phase response of a second-order system. | 6M           | CO5       | L5        |
| b)   | Explain about Design of Operational Amplifiers with Boundary conditions and Requirements.                        | 6M           | CO5       | L2        |

**OR**

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|-------|--|----|-----|----|
| 10.a) | Discuss about Cascoding of the first stage of the two-stage Operational Amplifier. | 6M | CO5 | L3 |
| b)    | Define CMRR and explain Configuration for simulating the common-mode gain.         | 6M | CO5 | L3 |

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