Course Code: D2515701

BONAM VENKATA CHALAMAYYA INSTITUTE OF TECHNOLOGY & SCIENCE

(AUTONOMOUS)

I – M. Tech I - Semester Regular Examinations (BR25), Feb - 2026

Digital CMOS Circuit Design (VLSI)

Time: 3 hours Max. Marks: 60

Answer any Five Questions One Question from One UNIT
ALL the Questions Carry Equal Marks

	UNIT-I	**Marks**	**CO**	**BL**
1.a)	Explain static and dynamic characteristics of an n-channel enhancement MOSFET with neat diagrams.	6M	CO1	BL5
b)	Describe the steps involved in converting a stick diagram to a full layout diagram for a CMOS inverter.	6M	CO1	BL3
	OR			
2.a)	Explain how transistor sizing affects the switching threshold and noise margins of a CMOS inverter.	6M	CO1	BL5
b)	Draw the stick diagram of a CMOS inverter and explain the representation of NMOS, PMOS, and interconnections.	6M	CO1	BL5
	UNIT-II	**Marks**	**CO**	**BL**
3.a)	Describe the use of logical effort in sizing gates for minimum delay in a multi-stage logic path.	6M	CO2	BL3
b)	Discuss the problems in dynamic logic and suggest remedies.	6M	CO2	BL2
	OR			
4.a)	Explain dynamic properties of CMOS gates and the factors affecting them.	6M	CO2	BL5
b)	Explain the techniques used to reduce interconnect delay.	6M	CO2	BL5
	UNIT-III	**Marks**	**CO**	**BL**
5.a)	Explain the principle of operation of a dynamic register implemented using dynamic latches.	6M	CO3	BL5
b)	What is pipelining in digital circuits? Explain how pipelining improves throughput with a suitable example.	6M	CO3	BL5
	OR			
6.a)	What are non-bistable sequential circuits? Give examples and explain their principle of operation.	6M	CO3	BL5
b)	Discuss timing issues in sequential circuits.	6M	CO3	BL2
	UNIT-IV	**Marks**	**CO**	**BL**
7.a)	Explain the operation of a ripple-carry adder. Discuss its advantages and limitations.	6M	CO4	BL5
b)	Describe the design of an accumulator that supports load, clear, and accumulate operations.	6M	CO4	BL3
	OR			

8.a)	What is a barrel shifter? Draw and explain the architecture of a barrel shifter using multiplexers.	6M	CO4	BL5
b)	What is a data path in a digital system? Explain the main components of a typical arithmetic data path with a neat block diagram.	6M	CO4	BL5

	UNIT-V	Marks	CO	BL
9.a)	Distinguish between static RAM (SRAM) and dynamic RAM (DRAM)	6M	CO5	BL2
b)	Explain memory architectures used in VLSI systems with neat block diagrams.	6M	CO5	BL5

OR

10.a)	Draw the circuit diagram of a 6-transistor (6T) CMOS SRAM cell and explain its operation during READ and WRITE cycles.	8M	CO5	BL5
b)	Define the function of a sense amplifier in memory.	4M	CO5	BL1

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