Course Code: D25157B0

BONAM VENKATA CHALAMAYYA INSTITUTE OF TECHNOLOGY & SCIENCE

(AUTONOMOUS)

I – M. Tech I - Semester Regular Examinations (BR25), Feb - 2026

VLSI Architectures (VLSI)

Time: 3 hours | Max. Marks: 60

Answer any Five Questions One Question from One UNIT
ALL the Questions Carry Equal Marks

	UNIT-I	**Marks**	**CO**	**BL**
1.a)	Compare memory-to-memory architecture and load/store architecture in CISC design.	8M	CO1	BL2
b)	Explain about the major factors affecting CPU performance.	4M	CO1	BL3
	OR			
2.	Discuss about the Multiply–Accumulate (MAC) instructions, Harvard architecture and Special addressing modes of DSP processors.	12M	CO1	BL2
	UNIT-II	**Marks**	**CO**	**BL**
3.a)	Draw the block diagram of the single-cycle datapath of a RISC processor and explain the execution of R-type and branch instructions.	6M	CO2	BL2
b)	Explain in detail the datapath execution of load (LW) and store (SW) instructions.	6M	CO2	BL2
	OR			
4.a)	Discuss the limitations of single-cycle processors and explain why this design is inefficient for modern processors.	6M	CO2	BL3
b)	Explain the role of various temporary registers in the multicycle datapath.	6M	CO2	BL3
	UNIT-III	**Marks**	**CO**	**BL**
5.a)	Explain the transformation of single-cycle Datapath into a pipelined Datapath by highlighting the important modifications.	6M	CO3	BL4
b)	Explain the role of the following Forwarding Unit in pipelined processors.	6M	CO3	BL3
	OR			
6.a)	Define structural hazards and explain their generation in pipelined processors.	6M	CO3	BL2
b)	Explain the delayed branch technique and its advantages and disadvantages.	6M	CO3	BL2
	UNIT-IV	**Marks**	**CO**	**BL**
7.a)	Explain the concept of thread-level parallelism (TLP) and its importance in multiprocessor design.	6M	CO4	BL3
b)	Explain the Mesh interconnection network topologies with diagrams.	6M	CO4	BL2
	OR			
8.a)	With a suitable example, explain the construction of a Data Flow Graph for a DSP algorithm and discuss its advantages.	6M	CO4	BL2
b)	Describe the Maximum Cycle Mean (MCM) algorithm for computing iteration bound in detail.	6M	CO4	BL2

	UNIT-V	Marks	CO	BL
9.a)	Discuss the concept of parallel processing in DSP systems and explain its advantages and limitations.	6M	CO5	BL3
b)	Discuss the effect of pipelining on throughput, latency, and hardware complexity in FIR filter implementations.	6M	CO5	BL4
	OR			
10.a)	Explain the folding transformation and describe the concept of folding factor and folding sets.	6M	CO5	BL3
b)	Discuss the retiming algorithm and its importance in VLSI DSP optimization.	6M	CO5	BL2

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