I YEAR II SEMESTER					
D2525701	CMOS MIXED SIGNAL CIRCUIT DESIGN	L	T	P	C
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Course Outcomes: At the end of the course, student will be able to

		Knowledge Level (K)#
CO1	Understand the necessity of mixed signal systems	K2
CO2	Analyze Op-Amp to meet the mixed signal specifications	K4
CO3	Design CMOS comparators to meet the high-speed requirements of digital circuitry	K5
CO4	Develop efficient data converter circuits for mixed signal systems	K4

#Based on suggested Revised BTL

Mapping of course outcomes with program outcomes

CO	PO1	PO2	PO3	PO4	PO5	PO6
CO1	M	L	M	M	M	H
CO2	L	L	M	H	M	H
CO3	M	M	M	H	H	H
CO4	M	L	M	H	H	H

Unit	Syllabus	Contact Hours
UNIT - I	Two-Stage OP-AMP Design :Parasitic Effects on Design of Two-Stage OP-AMP, Wide-Swing Cascode Current Mirrors, Design of Rugged Biasing Circuit with Temperature-Independent Compensation, Challenges in Mixed-Signal Circuit Design. Switched Capacitor Circuits : Constituents: Op-Amp, Capacitors, Switches, Non-overlapping Clocks; Basic Operation and Analysis, Resistor Equivalence of a Switched Capacitor, Parasitic-Sensitive Integrator, Parasitic-Insensitive Integrators, Signal-Flow-Graph Analysis, Design of Filters Based on Switched Capacitor Circuits.	12
UNIT - I	Sample-and-Hold Circuit: Testing Sample and Holds, MOS Sample-and-Hold Basics, Examples of CMOS S/H Circuits, Charge-Injection Errors, Making Charge-Injection Signal Independent, Minimizing Errors Due to Charge-Injection, Effect of Offset and Application of Switched Capacitor Circuits to Minimize Offset Errors, Parasitic Effects.	12
UNIT - III	Comparators: Ideal Comparator, Practical Model of Comparator, Resolving Capability, Propagation Delay, Small Signal Analysis, Conditions for Slewing, Evaluation of Propagation Delay for Single Pole and Two Pole Comparators, Design of Linear Response Comparators, Slew-Rate Limited Comparators, Comparators with Positive Feedback, Analysis of Latched Comparators, Architecture of	12

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	High-Speed Comparators, Self-Biased Comparators, Push Pull Comparators.	
UNIT - IV	Data Converters : Classification, Ideal D/A Converter, Ideal A/D Converter, Quantization Noise: Deterministic and Stochastic Approach, Signed Codes, Performance Limitations: Resolution, Offset and Gain Error, Accuracy and Linearity, Integrating Converters, Design of Successive-Approximation Converters, DAC-Based and Charge-Redistribution SAR, Interleaved, Pipelined, Flash, Principles of Sigma-Delta ADC, Testing of Data Converters.	12
UNIT - V	PLL and Oscillators : Basic PLL Architecture, VCO, Divider, Phase Detector, Loop Filter, PLL in Lock, Linearized Small-Signal Analysis, Second-Order PLL Model, Limitations, PLL Characterization and Design Example, Jitter and Phase Noise: Period Jitter, Cycle Jitter, Adjacent Period Jitter, Spectral Representations and PDF of Jitter, Ring and LC Oscillators, Phase Noise in Oscillators and PLLs.	12
	Total	60

TEXT BOOKS:

1. David Johns, Tony Chan Carusone and Kenneth Martin, Analog Integrated Circuit Design, Wiley, 2012, 2nd Edition.
2. Behzad Razavi, Design of Analog CMOS Integrated Circuits"McGraw Hill Education, 2017, 2nd Edition.
3. R.JacobBaker,CMOS:Mixed-SignalCircuitDesign,Wiley,2008,2nd Edition.

REFERENCE BOOKS:

1. Roubik Gregorian and Gabor C. Temes, Analog MOS integrated circuits for signal processing, Wiley, 1986.
2. Roubik Gregorian, Introduction to CMOS Op-Amps and Comparators, Wiley, 2008.
3. RuiPauloda Silva Martins and Pui-InMak,"Analog and Mixed-Signal Circuits in Nano scale CMOS", Springer, 2024.

Other Suggested Readings:

- NPTELCourses(https://onlinecourses.nptel.ac.in/noc22_ee34/preview)

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