



**BONAM VENKATA CHALAMAYYA INSTITUTE OF TECHNOLOGY &
SCIENCE
(AUTONOMOUS)**
(Approved by AICTE, Permanently Affiliated to JNTUK, Kakinada, Accredited by NAAC with 'A' Grade)
DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

PROFESSIONAL ELECTIVE-IV

I YEAR II SEMESTER

D25257B3	NANO ELECTRONICS	L	T	P	C
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Course Outcomes: At the end of the course, student will be able to

		Knowledge Level (K)#
CO1	To understand the basic science behind the design and fabrication of nano scale systems	K2
CO2	To understand and formulate new engineering solutions for current problems and competing technologies for future applications	K2
CO3	To be able make inter disciplinary projects applicable to wide areas by clearing and fixing the boundaries in system development	K3
CO4	To gather detailed knowledge of the operation of fabrication and characterization devices to achieve precisely designed systems	K4
CO5		

#Based on suggested Revised BTL

Mapping of course outcomes with program outcomes

CO/PO	PO1	PO2	PO3	PO4	PO5	PO6
CO1	M	L	M	M	H	H
CO2	M	L	M	M	H	H
CO3	M	L	M	M	H	H
CO4	M	L	M	M	H	H

Unit	Syllabus	Contact Hours
UNIT I	Overview: Nano devices, Nano materials, Nano device characterization, Definition of Technology node, MOS capacitor, MOS Scaling theory, Moore's Law and Koomey's law.	12
UNIT II	Issues in scaling MOS transistors: Short channel effects, Description of a typical 65 nm CMOS technology, Role of interface quality and related process techniques, Gate oxide thickness, scaling trend, SiO ₂ vs High-k gate dielectrics, Integration issues of high-k, Interface states, bulk charge, band offset, stability, reliability - Qbd high field, possible candidates, CV and IV techniques, Transport in Nano MOSFET, velocity saturation, ballistic transport, injection velocity, velocity overshoot. Metal gate transistor: Motivation, requirements, Integration Issues.	12
UNIT III	Non-classical MOS transistor: Requirements and Novel devices - SOI: PD-SOI and FD-SOI, Ultra-thin body SOI, Double gate transistors, integration issues. Vertical transistors - FinFET and	12

Shreeni

Dr. T.S.S. PHANI
B.E, M.Tech, Ph.D, MIETE, MIAENG
Professor & HOD
Department of ECE
BVCITS, Batlapalem



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UNIT IV	Novel devices: Tunnel FET, Negative-Capacitance (NC) FET. Metal source/drain junctions - Properties of Schottky junctions on Silicon, Germanium and compound semiconductors - Work function pinning.	12
UNIT V	Emerging Nano MOSFETs: Strain, quantization, Advantages of Germanium over Silicon, PMOS versus NMOS. Compound semiconductors MOSFETs in the context of channel quantization and strain, Heterostructure MOSFETs, exploiting novel materials, strain, quantization. CNT, Graphene, Nanotubes, Nanorods and other nano-structures.	12
Total		60

Text Books:

1. Kenneth J. Klabunde and Ryan M. Richards, "Nanoscale Materials in Chemistry", 2nd edition, John Wiley and Sons, 2009.
2. I Gusev and A A Rempel, "Nanocrystalline Materials", Cambridge International Science Publishing, 1st Indian edition by Viva Books Pvt. Ltd. 2008.
3. B. S. Murty, P. Shankar, Baldev Raj, B. B. Rath, James Murday, "Nanoscience and Nanotechnology", Tata McGraw Hill Education 2012.

Reference Books:

1. Bharat Bhushan, "Springer Handbook of Nanotechnology", Springer, 3rd edition, 2010.
2. Kamal K. Kar, "Carbon Nanotubes: Synthesis, Characterization and Applications", Research Publishing Services; 1st edition, 2011, ISBN-13: 978-9810863975.

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