BONAM VENKATA CHALAMAYYA INSTITUTE OF TECHNOLGY & SCIENCE
(AUTONOMOUS)
(Approved by AICTE, Permanently Affiliated to JNTUK, Kakinada, Accredited by NAAC with 'A' Grade)
DEPARTMENTOFELECTRONICS AND COMMUNICATIONENGINEERING

I YEAR II SEMESTER					
D2525702	PHYSICAL DESIGN VERIFICATION	L	T	P	C
		3	1	0	4

Course Outcomes: At the end of the course, student will be able to

		Knowledge Level (K)#
CO1	Understand the relationship between design automation algorithms and Various constraints posed by VLSI fabrication and design technology	K2
CO2	Adapt the design algorithms to meet the critical design parameters.	K3
CO3	Identify layout optimization techniques and map them to the algorithms	K3
CO4	Develop proto-type EDA tool and test its efficacy	K4

#Based on suggested Revised BTL

Mapping of course outcomes with program outcomes

CO	PO1	PO2	PO3	PO4	PO5	PO6
CO1	M	L	M	H	H	M
CO2	L	M	M	H	M	M
CO3	M	M	M	H	H	L
CO4	H	M	H	H	M	M

Unit	Syllabus	Contact Hours
UNIT I	VLSI Design Cycle, Physical Design Cycle, Design Rules, Layout of Basic Devices, and Additional Fabrication. Design styles: Full Custom, Standard Cell, Gate Arrays, Field Programmable Gate Arrays, Sea of Gates and Comparison, System Packaging Styles, Multi-Chip Modules. Design Rules, Layout of Basic Devices, Fabrication Process and Its Impact on Physical Design, Interconnect Delay, Noise and Crosstalk, Yield and Fabrication Cost.	12
UNIT II	Factors, Complexity Issues and NP-hard Problems. Basic Algorithms (Graph and Computational Geometry): Graph Search Algorithms, Spanning Tree Algorithms, Shortest Path Algorithms, Matching Algorithms, Min-Cut and Max-Cut Algorithms, Steiner Tree Algorithms.	12
UNIT III	Basic Data Structures: Atomic Operations for Layout Editors, Linked List of Blocks, Bin Based Methods, Neighbour Pointers, Corner Stitching, Multi-Layer Operations.	12
UNIT IV	Graph Algorithms for Physical Design: Classes of Graphs, Graphs Related to a Set of Lines, Graphs Related to a Set of Rectangles, Graph Problems in Physical Design, Maximum Clique and Minimum Coloring, Maximum k-Independent Set Algorithm, Algorithms for Circle Graphs.	12

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UNIT V	Partitioning Algorithms: Design Style Specific Partitioning Problems, Group Migrated Algorithms, Simulated Annealing and Evolution. Floor Planning and Pin Assignment, Routing and Placement Algorithms.	12
	Total	60

Text Books:

1. Naveed Shervani, Algorithms for VLSI Physical Design Automation, 3rd Edition, Kluwer Academic, 1999.
2. Charles J Alpert, Dinesh P Mehta, Sachin S Sapatnekar, Handbook of Algorithms for Physical Design Automation, CRC Press, 2008

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