I YEAR II SEMESTER					
D2525703	VLSI TESTING & TESTABILITY	L	T	P	C
		3	1	0	4

Course Outcomes: At the end of the course, student will be able to

		Knowledge Level (K)#
CO1	Identify the significance of testable design	K3
CO2	Understand the concept of yield and identify the parameters influencing the same	K2
CO3	Specify fabrication defects, errors, and faults	K3
CO4	Implement combinational and sequential circuit test generation algorithms	K4
CO5	Identify techniques to improve fault coverage	K5

#Based on suggested Revised BTL

Mapping of course outcomes with program outcomes

CO	PO1	PO2	PO3	PO4	PO5	PO6
CO1	L	L	M	H	M	L
CO2	M	M	M	H	H	M
CO3	M	L	M	H	H	M
CO4	M	M	M	H	M	H
CO5	M	L	M	H	H	M

Unit	Syllabus	Contact Hours
UNIT I	Role of Testing in VLSI Design Flow, Testing at Different Levels of Abstraction, Fault, Error, Defect, Diagnosis, Yield. Types of Testing, Rule of Ten, Defects in VLSI Chip. Modelling Basic Concepts, Functional Modelling at Logic Level and Register Level, Structure Models, Logic Simulation, Delay Models. Various Types of Faults, Fault Equivalence and Fault Dominance in Combinational and Sequential Circuits.	12
UNIT II	Fault Simulation Applications, General Fault Simulation Algorithms: Serial and Parallel, Deductive Fault Simulation Algorithms.	12
UNIT III	Combinational Circuit Test Generation, Structural Vs Functional Test, ATPG, Path Sensitization Methods. Difference Between Combinational and Sequential Circuit Testing, Five and Eight Valued Algebra, Scan Chain-Based Testing Method.	12
UNIT IV	D-Algorithm Procedure, Problems. PODEM Algorithm, Problems on PODEM Algorithm. FAN Algorithm, Problems on FAN Algorithm. Comparison of D, FAN and PODEM Algorithms. Design for Testability, Ad-Hoc Design, Generic Scan-Based Design.	12

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UNIT V	Classical Scan-Based Design, System Level DFT Approaches. Test Pattern Generation for BIST, Circular BIST, BIST Architectures. Testable Memory Design: Test Algorithms, Test Generation for Embedded RAMs.	12
	Total	60

TEXT BOOKS:

1. M. Abramovici, M. Breuer, and A. Friedman, "Digital Systems Testing and Testable Design, IEEE Press, 1990.
2. M. Bushnell and V. Agrawal, "Essentials of Electronic Testing for Digital, Memory & Mixed-Signal VLSI Circuits", Kluwer Academic Publishers, 2000.

REFERENCE BOOKS:

1. Stroud,"A Designer's Guide to Built-in Self-Test", Kluwer AcademicPublishers,2002
2. V.Agrawal and S.C.Seth, Test Generation for VLSI Chips, Computer Society Press. 1989

Other Suggested Readings:

1. NPTELCourses(https://archive.nptel.ac.in/courses/117/105/117105137/)

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