Course Code: 23EC6T10

BONAM VENKATA CHALAMAYYA INSTITUTE OF TECHNOLOGY & SCIENCE

(AUTONOMOUS)

III-B.Tech II-Semester Regular Examinations (BR23), April/May - 2026

MICROPROCESSORS AND MICROCONTROLLERS (ECE)

Time: 3 hours Max. Marks: 70

Question Paper consists of Part-A and Part-B

*Answer **ALL** the question in **Part-A and Part-B***

PART–A (10X2 = 20M)

		Marks	CO	BL
1. a)	Explain any two differences between Harvard and Von Neumann architectures.	(2M)	CO1	BL2
b)	What is the size of the address bus and data bus in 8086?	(2M)	CO1	BL2
c)	What is the function of the PUSH and POP instructions?	(2M)	CO2	BL2
d)	List any four addressing modes of 8086	(2M)	CO2	BL2
e)	Draw the control register format of IO mode in 8255	(2M)	CO3	BL2
f)	What is meant by over run error in 8251 USART	(2M)	CO3	BL2
g)	What is the internal ROM and RAM capacity of Microcontroller	(2M)	CO4	BL2
h)	Draw the flag register of 8051 Microcontroller	(2M)	CO4	BL2
i)	Write any two salient features of ARM processor	(2M)	CO5	BL2
j)	What are the differences between RISC and CISC	(2M)	CO5	BL2

PART–B (5X10 = 50M)

2a.	Explain the internal architecture of 8086 microprocessor with a neat diagram	5(M)	CO1	BL2
b.	Compare the differences between Microprocessors & Microcontrollers	5(M)	CO1	BL3
	(OR)			
3a.	Demonstrate the register organization of 8086	5(M)	CO1	BL2
b.	Compare the Harvard and Von Neumann architectures with suitable examples	5(M)	CO1	BL2

4a.	Write an assembly language program to find the largest number of an array	5(M)	CO2	BL3
b.	Explain about the assembler directives of 8086 microprocessor with examples	5(M)	CO2	BL2
	(OR)			
5a.	Draw the interrupt vector table of 8086 microprocessor and explain its operation in detail	5(M)	CO2	BL2
b.	Explain the following instructions of 8086 i). ROL ii). LOCK iii). CALL iv). AAA	5(M)	CO2	BL2

6a.	With a neat block diagram ,explain in detail the internal architecture of 8255	5(M)	CO3	BL2

b.	Interface ADC 0808 with 8086 using 8255 ports .Use port A of 8255 for transferring digital data output of ADC to the CPU and port C for control signals .Assume that an analog input is present at input 2 of ADC and a clock input of suitable frequency is available for ADC	5(M)	CO3	BL3
	(OR)			
7a.	Draw the block diagram of USART 8251 and explain its operation	5(M)	CO3	BL2
b.	Design a 74LS138 decoder to generate select lines for 4 memory devices. Each memory device has a capacity of 16 KB. The address range of total memory is from 40000H to 4FFFFH. Assuming the processor is of 20 bit address capacity	5(M)	CO3	BL3

8a.	Explain in detail Timer modes of operation with necessary registers of 8051 microcontroller	5(M)	CO4	BL2
b.	Describe the internal architecture of the 8051 Microcontroller	5(M)	CO4	BL2
	(OR)			
9a.	Explain the addressing modes of 8051 Microcontroller.	5(M)	CO4	BL2
b.	Explain the following i) SCON ii) PCON	5(M)	CO4	BL2
10a.	Describe in detail the modes of operation in ARM processor	5(M)	CO5	BL2
b.	Write about the flag register in ARM Processor	5(M)	CO5	BL2
	(OR)			
11a.	Explain the internal architecture of ARM Processor	5(M)	CO5	BL2
b.	Discuss the ARM instruction pipeline and its benefits	5(M)	CO5	BL2

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