Course Code: 23EC6T09

BONAM VENKATA CHALAMAYYA INSTITUTE OF TECHNOLOGY & SCIENCE

(AUTONOMOUS)

III - B.Tech II-Semester Regular Examinations (BR23), April/May - 2026

VLSI DESIGN (ECE)

Time: 3 hours Max. Marks: 70

Question Paper consists of Part-A and Part-B

*Answer **ALL** the question in **Part-A and Part-B***

PART–A (10X2 = 20M)

		Marks	CO	BL
1. a)	List out different IC technologies including number of gates.	(2M)	CO1	L1
b)	Why is VLSI design process presented in NMOS only? Justify with an example?	(2M)	CO1	L1
c)	Explain about the constraints in choice of layers.	(2M)	CO2	L2
d)	Differentiate two scaling techniques.	(2M)	CO2	L4
e)	Define long channel effect and short channel effect.	(2M)	CO3	L1
f)	Explain about channel length modulation.	(2M)	CO3	L2
g)	Write about pass transistor and pass transistor gates.	(2M)	CO4	L1
h)	Draw and explain the basic structure of a dynamic CMOS design.	(2M)	CO4	L3
i)	What is the need of a FPGA? And write its applications.	(2M)	CO5	L1
j)	Explain high k metal gate.	(2M)	CO5	L2

PART–B (5X10 = 50M)

2a.	Derive the relationship between drain to source current Ids versus drain to source voltage Vds in a non-saturated and a saturated region.	5M	CO1	L3
2b.	Design schematic, stick diagram and MOS layout of the following function using CMOS logic f=($(A+B)(C+D)$)′	5M	CO1	L3
	(OR)			
3a.	Derive the equations for Ids of an n-channel enhancement MOSFET operating in Non-saturated region and saturated region?	5M	CO1	L3
3b.	Explain 2 μm Double Metal, Double Poly CMOS / Bi-CMOS Rules.	5M	CO1	L2

4a.	Derive the propagation delay for NMOS AND CMOS inverter?	5M	CO2	L3
4b.	Describe three sources of wiring capacitances. Explain the effect of wiring capacitance on the performance of a VLSI circuit.	5M	CO2	L3
	(OR)			
5a.	What is meant by sheet resistance Rs? Explain the concept of Rs applied to MOS transistors.	5M	CO2	L2

5b.	b) Derive the expressions for rise time and fall time in the case of CMOS inverter.	5M	CO2	L2

6a.	Explain the small signal model for common source stage and sketch the drain current and trans conductance of transistor as a function of the input voltage?	5M	CO3	L2
6b.	Briefly discuss about CS stage with diode connected load and derive an expression for voltage gain.	5M	CO3	L4
	(OR)			
7a.	List out different biasing styles of MOSFET and explain.	5M	CO3	L2
7b.	Explain briefly about body bias effect with neat diagrams?	5M	CO3	L2

8a.	What are the Issues in Dynamic Design and explain.	5M	CO4	L2
8b.	Draw the Master-slave positive edge-triggered register using multiplexers and explain the operation?	5M	CO4	L3
	(OR)			
9a.	What is pipelining? Explain the operation of two-phase pipelined circuit using dynamic registers?	5M	CO4	L2
9b.	Explain about static, dynamic and domino CMOS logics with examples.	5M	CO4	L2

10a.	Explain the step by step approach of FPGA design process on Xilinx environment.	5M	CO5	L2
10b.	Write about Drain Induced Barrier Lowering effect in nMOS transistor? Explain with neat sketch.	5M	CO5	L2
	(OR)			
11a.	Explain the following terms: i) LUT ii) CLB iii) IOB iv) Switch matrix	5M	CO5	L2
11b.	Explain the following terms in detail (a) Fin-FET (b)TFET	5M	CO5	L2

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