Course Code: 23EC6T09

BONAM VENKATA CHALAMAYYA INSTITUTE OF TECHNOLOGY & SCIENCE

(AUTONOMOUS)

III - B.Tech II-Semester Regular Examinations (BR23), MAY - 2026

VLSI DESIGN (ECE)

Time: 3 hours Max. Marks: 70

Question Paper consists of Part-A and Part-B
*Answer **ALL** the question in **Part-A andPart-B***

PART–A (10X2 = 20M)

		Marks	CO	BL
1. a)	What is the role of photolithography in IC fabrication.	2M	CO1	L1
b)	Define threshold voltage of a MOSFET.	2M	CO1	L1
c)	List the limitations of scaling.	2M	CO2	L1
d)	Explain sheet resistance. Give its formula and unit.	2M	CO2	L2
e)	Define transconductance of a MOSFET and give its expression.	2M	CO3	L1
f)	Explain the purpose of biasing in analog circuits.	2M	CO3	L2
g)	Draw CMOS NAND gate circuit.	2M	CO4	L1
h)	Briefly discuss issues in dynamic design.	2M	CO4	L2
i)	List the advantages of Fin FET	2M	CO5	L1
j)	Draw FPGA design flow.	2M	CO5	L1

PART–B (5X10 = 50M)

2a.	Explain the VLSI design flow with neat diagram	5M	CO1	L2
2 b.	Derive the pull-up to pull-down ratio for a NMOS inverter driven by another NMOS inverter	5M	CO1	L4
	(OR)			
3 a.	Explain the concept of design rules in VLSI layout	5M	CO1	L2
3 b.	Explicate the NMOS enhancement mode fabrication process.	5M	CO1	L3
4a	Calculate the ON resistance from V_{DD} to GND for the NMOS and CMOS inverter circuits	5M	CO2	L2
4 b.	How does depletion regions around source and drain are affected due to scaling down the device dimensions? Explain.	5M	CO2	L3
	(OR)			
5a	What is the problem of driving large capacitive loads? Explain a method to drive such load.	5M	CO2	L2
5 b.	Determine the scaling factors of the following a. Power dissipation per gate b. Maximum operating frequency c. Gate capacitance per unit area.	5M	CO2	L4

6 a.	With neat circuit diagram demonstrate the operation of common source amplifier.	5M	CO3	L3
6 b.	Briefly explain about current sinks and sources.	5M	CO3	L2
	(OR)			
7.	Describe the regions of operation of MOSFET in detail.	10M	CO3	L3
8 a.	Explain the importance of pass transistor logic along with example.	5M	CO4	L2
8 b.	Explain CMOS rationed logic in detail.	5M	CO4	L2
	(OR)			
9.	Design a full adder circuit using CMOS logic.	10 M	CO4	L4
10 a	Draw and explain the basic architecture of FPGA.	5M	CO5	L2
10 b	Briefly discuss about FPGA technologies.	5M	CO5	L2
	(OR)			
11 a.	Differentiate between Fin FET and TFET	5M	CO5	L4
11 b.	Write a short notes on metal gate technology	5M	CO5	L2

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